REMARKS

Reconsideration of the application as amended herein is respectfully requested. Claims-1-4 have been cancelled. Claims 5-9 have been added. After amendment, claims 5-9 remain.

Specification Objections

The Office Action has objected to the specification. Applicant has amended the application to place the serial numbers of the co-pending applications in the appropriate locations.

Claim Rejections - 35 U.S.C. § 112

The Office Action has rejected claims 1-4 under 35 U.S.C. § 112, first and second paragraph. Applicant respectfully traverses these rejections, as it believes that new claims 5-9 (1) particularly point out and distinctly claim the subject matter they cover and (2) are enabled. In particular, the Office Action argues that the architecture of the modules found in cancelled claims 1-4 is unclear. Applicant points out that the newly presented claims make it clear that each module is comprised of a number of clusters and that these clusters are comprised a number of processors. Thus, for each module, there can be a cluster comprised of, for example, four processors. See Fig. 2. As the specification makes clear, each module can have multiple clusters. See e.g., specification at page 5, lines 26-31.[1] It is noted that persons having ordinary skill in the art would recognize that an emulation engine can comprise more than one module. For example, see e.g., Fig. 7 of U.S. Patent No. 5,551,013, which was incorporated by reference into the present application.

[1] Note that this paragraph has been amended solely to make specific reference to issued patent No. 6,618,698, which is the "pending application" referred to in this citation.

Claim Rejections - 35 U.S.C. § 102(b)

The Office Action has rejected claims 1-4 under 35 U.S.C. § 102(b) as being anticipated by Staros. Applicant respectfully traverses this rejection. Firstly, Applicant has cancelled claims 1-4, thus rendering this rejection moot. Applicant respectfully submits that new claims 5-9 are not anticipated by Staros because Staros does not teach the use of processors that "execute logic gate functions from a logic design". The present claims define an apparatus used to verify the functionality of logic designs, which require that the processors be able to execute the logic functions present in the logic design. Staros teaches no such feature and in fact is directed to digital signal processing, which one having ordinary skill in the art would recognize does not have anything to do with verifying the functionality of a logic design. Moreover, Staros says nothing about organizing its digital signal processors into clusters, which is required by each of the claims.

In addition, and contrary to what is stated in the Office Action, Staros does not teach the use of a time division multiplexer for each cluster that is coupled to the read ports of the processors within that cluster. First, since Staros says nothing about clustering of processors, it cannot teach the use of a time division multiplexer for each cluster. Likewise, since Staros does not teach anything about clustering, all Staros can teach is the use of a time-multiplexed *bus* that is distributed throughout the integrated circuit. Staros does not teach the use of a time division multiplexer (as opposed to a bus) for use within each cluster.

Moreover, the claims of the present application require that the read ports *of the processors* be coupled to the time division multiplexer in each cluster. As seen in Fig. 4 of Staros, the read ports of the digital signal processor (reference numeral 102) are connected to a

memory device (reference numeral 104). Because of this, the memory device (reference numeral 102) in Staros is what is coupled to the time multiplexed bus. Thus, claim limitations requiring the read ports of the processors be coupled to the time division multiplexer are also missing from Staros. Thus, Applicant respectfully submits that all of the presently pending claims are allowable over Staros.

Based on the foregoing, Applicant respectfully submits that the subject application is in condition for allowance. Applicant therefore respectfully requests that the present application be allowed.

Should the Examiner have any questions or comments on the application, the undersigned can be reached at (650) 614-7660.

Respectfully submitted,
ORRICK, HERRINGTON & SUTCLIFFE LLP

Dated: November 29, 2004 By: _____
Jeffrey A. Miller
Reg. No. 35,287

Four Park Plaza, Suite 1600
Irvine, California 92614-2558
(650) 614-7660